

WHAT IS CLAIMED IS:

SUB 927

1 1. A method of monitoring the performance of a program being executed on
2 a computer system, comprising:
3 executing the program on a computer system, the program having object code
4 instructions;
5 at intervals interrupting execution of the program, including delivering a first
6 interrupt; and
7 in response to at least a subset of the first interrupts, determining a latency
8 associated with a particular object code instruction, storing the latency in a first
9 database, the particular object code instruction being executed by the computer such
10 that the program remains unmodified.

1 2. The method of claim 1 wherein said determining the latency includes:
2 determining an initial value of a cycle counter;
3 performing the particular object code instruction;
4 determining a final value of the cycle counter; and
5 determining the latency based on the initial value and the final value.

1 3. The method of claim 2 further comprising:
2 executing at least one instruction selected from the set consisting of (A) an
3 instruction for ensuring that the particular object code instruction is performed after the
4 initial value of the cycle counter is determined, and (B) an instruction for ensuring that
5 the particular object code instruction is performed before the final value of the cycle
6 counter is determined.

1 4. The method of claim 2 further comprising:
2 applying an adjustment to the final value.

1 5. The method of claim 1 wherein said determining the latency includes:
2 determining an initial value of an event counter;
3 performing the particular object code instruction;

1 determining a final value of the event counter; and
2 determining the latency based on the initial value and the final value.
3

4 6. The method of claim 1 wherein the particular object code instruction has
5 a variable execution time.

1 7. The method of claim 1 wherein the particular object code instruction is a
2 memory access instruction.

1 8. The method of claim 1 wherein the computer system includes a plurality
2 of memory units, each memory unit of the plurality of memory units having a different
3 range of access times, and further comprising:

4 associating the particular object code instruction with a memory unit in
5 accordance with the latency and the range of access times for the memory unit.

1 9. The method of claim 1 wherein said determining the latency includes:
2 determining an initial value of a cycle counter;
3 executing a first dependent instruction to provide a predetermined execution
4 order;

5 performing the particular object code instruction;
6 executing a second dependent instruction to provide the predetermined
7 execution order;

8 determining a final value of the cycle counter; and
9 determining the latency based on the initial value and the final value.

1 10. The method of claim 9 wherein the first and second dependent
2 instructions are memory barrier instructions.

1 11. The method of claim 1 wherein said determining includes:
2 identifying at least one issue block of instructions; and
3 interpreting the instructions of the at least one issue block;
4 wherein said particular object code instruction is in the issue block.

1 12. The method of claim 11 wherein said interpreting emulates a machine
2 language instruction set of the computer system.

1 13. The method of claim 11 wherein said interpreting updates a state of the
2 interrupted program as though each interpreted instruction had been directly executed
3 by the computer system.

1 14. A computer program product for sampling latency of a computer program
2 having object code instructions while the object code instructions are executing without
3 modifying the computer program, the computer program product for use in conjunction
4 with a computer system, the computer program product comprising a computer
5 readable storage medium and a computer program mechanism embedded therein, the
6 computer program mechanism comprising:

7 one or more instructions to deliver interrupts at intervals during execution of the
8 program, including delivering a first interrupt;

9 one or more instructions to determine a latency value for a particular object code
10 instruction; and

11 one or more instructions to, in response to at least a subset of the first interrupts,
12 store the latency value for the particular object code instruction in a first database.

1 15. The computer program product of claim 14 wherein said one or more
2 instructions to determine the latency value include instructions to:

3 determine an initial value of a cycle counter;

4 perform the particular object code instruction;

5 determine a final value of the cycle counter; and

6 determine the latency based on the initial value and the final value.

1 16. The computer program product of claim 14 further comprising at least one
2 instruction selected from the set consisting of (A) an instruction for ensuring that the
3 particular object code instruction is performed after the initial value of the cycle counter

1 is determined, and (B) an instruction for ensuring that the particular object code
2 instruction is performed before the final value of the cycle counter is determined.

1 17. The computer program product of claim 15 further comprising one or
2 more instructions to apply an adjustment to the final value.

1 18. The computer program product of claim 14 wherein said one or more
2 instructions to determine the latency value include instructions to:
3 determine an initial value of an event counter;
4 perform the particular object code instruction;
5 determine a final value of the event counter; and
6 determine the latency based on the initial value and the final value.

1 19. The computer program product of claim 14 wherein the particular object
2 code instruction has a variable execution time.

1 20. The computer program product of claim 14 wherein the particular object
2 code instruction is a memory access instruction.

1 21. The computer program product of claim 14 wherein the computer system
2 includes a plurality of memory units, each memory unit of the plurality of memory units
3 having a different range of access times, and further comprising one or more
4 instructions that associate the particular object code instruction with a memory unit in
5 accordance with the latency value and the range of access times for the memory unit.

1 22. The computer program product of claim 14 wherein said one or more
2 instructions to determine the latency value include:
3 one or more instructions to determine an initial value of a cycle counter;
4 a first dependent instruction to provide a predetermined execution order;
5 the particular object code instruction;
6 a second dependent instruction to provide the predetermined execution order;
7 one or more instructions to determine a final value of the cycle counter; and

1 one or more instructions to determine the latency value based on the initial value
2 and the final value.

1 23. The computer program product of claim 22 wherein the first and second
2 dependent instructions are memory barrier instructions.

1 24. The computer program product of claim 14 wherein said instructions to
2 determine include:

3 one or more instructions that identify at least one issue block of instructions; and
4 an interpreter to interpret the instructions of the at least one issue block;
5 wherein said particular object code instruction is in the issue block.

1 25. The computer program product of claim 24 wherein the interpreter
2 emulates a machine language instruction set of the computer system.

1 26. The computer program product of claim 24 wherein the interpreter
2 updates a state of the interrupted program as though each interpreted instruction had
3 been directly executed by the computer system.

1 27. A computer system comprising:
2 a processor for executing instructions; and
3 a memory storing instructions including:

4 one or more instructions to deliver interrupts at intervals during execution of the
5 program, including delivering a first interrupt;

6 one or more instructions to determine a latency value for a particular object code
7 instruction; and

8 one or more instructions to, in response to at least a subset of the first interrupts,
9 store the latency value for the particular object code instruction in a first database.

1 28. The computer system of claim 27 wherein said one or more instructions
2 to determine the latency value include instructions to:

3 determine an initial value of a cycle counter;

1 perform the particular object code instruction;
2 determine a final value of the cycle counter; and
3 determine the latency based on the initial value and the final value.

1 29. The computer system of claim 27 wherein the memory further comprises
2 at least one instruction selected from the set consisting of (A) an instruction for
3 ensuring that the particular object code instruction is performed after the initial value of
4 the cycle counter is determined, and (B) an instruction for ensuring that the particular
5 object code instruction is performed before the final value of the cycle counter is
6 determined.

1 30. The computer system of claim 28 wherein the memory further comprises
2 one or more instructions to apply an adjustment to the final value.

1 31. The computer system of claim 27 wherein said one or more instructions
2 to determine the latency value include instructions to:
3 determine an initial value of an event counter;
4 perform the particular object code instruction;
5 determine a final value of the event counter; and
6 determine the latency based on the initial value and the final value.

1 32. The computer system of claim 27 wherein the particular object code
2 instruction has a variable execution time.

1 33. The computer system of claim 27 wherein the particular object code
2 instruction is a memory access instruction.

1 34. The computer system of claim 27 further comprising:
2 a plurality of memory units, each memory unit of the plurality of memory units
3 having a different range of access times, and

1 wherein the memory further comprises one or more instructions that associate
2 the particular object code instruction with a memory unit in accordance with the latency
3 value and the range of access times for the memory unit.

1 35. The computer system of claim 27 wherein said one or more instructions
2 to determine the latency value include:
3 one or more instructions to determine an initial value of a cycle counter;
4 a first dependent instruction to provide a predetermined execution order;
5 the particular object code instruction;
6 a second dependent instruction to provide the predetermined execution order;
7 one or more instructions to determine a final value of the cycle counter; and
8 one or more instructions to determine the latency value based on the initial value
9 and the final value.

1 36. The computer system of claim 36 wherein the first and second dependent
2 instructions are memory barrier instructions.

1 37. The computer system of claim 27 wherein said instructions to determine
2 include:
3 one or more instructions that identify at least one issue block of instructions; and
4 an interpreter to interpret the instructions of the at least one issue block;
5 wherein said particular object code instruction is in the issue block.

1 38. The computer system of claim 37 wherein the interpreter emulates a
2 machine language instruction set of the computer system.

1 39. The computer system of claim 37 wherein the interpreter updates a state
2 of the interrupted program as though each interpreted instruction had been directly
3 executed by the computer system.